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INTEGRATED INJECTION LOGIC (I^2L)

Comparative and Design Trade-off Evaluation

Mission Research Corporation
P.O. Box 1209
La Jolla, California 92038

7 December 1976

Topical Report for Period May 1976 — December 1976

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Electrical parameters and radiation susceptibility of integrated injection logic (I^2L) microcircuit circuit technology are reviewed. Comparisons are drawn between I^2L and other contemporary LSI microcircuit technologies such as TTL, Schottky-clamped TTL, ECL, p-MOS, n-MOS, CMOS and CMOS/SOS. Performance parameters considered include cell density, switching speed,

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20. ABSTRACT (Continued)

power dissipation, speed-power product, output drive capability and temperature range. Radiation effects considered are those of neutron damage, long-term ionization damage, electrical pulsed overstress damage and transient photoresponse.

Trade-offs in electrical performance parameters and radiation susceptibility are suggested for "conventional" I^2L design. Critical design considerations in I^2L are electrical switching response, noise margin and neutron damage susceptibility. On the other hand, I^2L is of potential major advantage in the parameters of power dissipation, temperature range, long-term ionization damage susceptibility and transient photoresponse.

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SECTION 1

1.0 INTRODUCTION

1.1 Purpose

This report presents (1) a comparison of I^2L in contrast to other developing bipolar and MOS LSI technologies, (2) considerations in the trade-off of electrical performance and radiation hardness with variation of I^2L design parameters, and (3) comments on the probable evolution of semiconductor LSI technologies. This report is a supplement to an NWSC evaluation of I^2L, which includes characterization of advanced microcircuits and evaluation of hardened system microcircuit performance requirements.

1.2 Scope

The comparative evaluation is defined by the technologies considered and the electrical performance parameters selected as the basis of comparison. Microelectronic technologies to be considered include:

transistor-transistor logic (TTL),

Schottky-clamped TTL (S/C TTL),

radiation-hardened TTL (R/H TTL),

emitter-coupled logic (ECL),

integrated injection logic (I^2L),

p-MOS,

n-MOS,

CMOS, and

CMOS/SOS.

Performance parameters considered as basis for comparison include:

cell density,

switching speed,

power dissipation (static and dynamic),

speed-power product,

output drive capability,

noise immunity, and

temperature range

for electrical performance parameters, and

neutron damage susceptibility,

long-term ionization damage susceptibility,

transient logic upset, and

electrical puised overstress susceptibility

for nuclear radiation hardness.

In the trade-off evaluation, critical design parameters of the basic I^2L inverter are considered in terms of electrical performance and

radiation hardness. Variation of design parameters for increasing hardness are considered in terms of possible compromise of electrical perfomrance parameters. This conpromise, when present, will force a trade-off between performance and hardness and suggests the possibility of different design criteria for different radiation specifications.

Evolution of semiconductor technologies is discussed in terms of those that seem most promising at the moment. These include high density n-MOS (which leads into CCD arrays), CMOS/SOS, and advanced I^2L structures.

1.3 Background

Integrated Injection Logic (or Merged Transistor Logic) was originally proposed in 1972 by researchers at IBM-Boeblingen for application in a high-density, low-power memory[1], and by researchers at Phillips-Eindhoven for application in light-powered instrumentation.[2] Performance characteristics of I^2L arrays were exclusively published by IBM and Phillips through 1974 in several technical papers.[3-7] In 1974, the first papers were published on the design considerations and modeling of I^2L logic cells[8-11], as well as the first suggestion for performance improvement by process modification (oxide-isolation).[12] Results were presented at the IEEE Electron Device Meeting which examined the sensitivity of the I^2L inverter gain to the characteristics of the n^+ isolation collar[13], and the first major structural variation of the structure (substrate-fed-logic) was proposed as a performance advantage.[14] Early in 1975, Texas Instruments revealed its major development effort in I^2L by the announcement of the SBP 0400 microprocessor.[15]

There have been extensive publications on I^2L and its variations from 1975 to the present. These publications generally fall into categories of (1) product design and performance considerations[17,25,26,31]

(2) variations on the basic structure to improve electrical performance (e.g., the use of Schottky diodes,[16,21,27] substrate-fed-logic,[26] vertical injection logic,[32] and folded-collector logic[33]), (3) modeling of the baseline I^2L structure,[18,30,34] and (4) characterization of radiation effects on available test structures.[19,23,24,28,36,37] There are also a few papers that provide data in a comparison of competitive LSI technologies,[15,29,38] as well as criteria that can be used in comparison.[35] Excluding the earliest papers, most published results on I^2L consider it only as a digital array rather than as a digital pocket in a junction-isolated digital analog array. The process considerations in combined digital/analog arrays are complex,[31] and have yet to result in a commercial product.

DoD involvement in the development of I^2L technology has been relatively modest. ECOM supported a design study in an I^2L frequency synthesizer development as well as a follow-on effort to define performance/yield trade-offs in LSI shift-register arrays.[40] Programs in characterization of radiation effects on available test structures have been supported since 1974 by DNA through a Northrop contract,[41] and by the Naval Weapon Support Center with Naval Special Project Office support. More recently, these studies have been supplemented by IR&D studies at General Electric, Boeing, Fairchild, and Harris Semiconductor.

1.4 Summary

Comparison of evolving LSI technologies is difficult because of the wide variations in the nature of competing technologies and in requirements of potential applications. Results of comparing I^2L to other LSI technologies are summarized subjectively in Table 1.1. These results are supported quantitatively in the body of this report. From this subjective comparison, it is clear that I^2L is a superior LSI technology in terms of cell density, power dissipation, speed-power product, and transient logic upset level. I^2L is better in switching speed, output drive capability,

temperature range, long-term ionization susceptibility, high dose rate survivability, and electrical pulsed overstress susceptibility than most MOS technologies, but is generally weaker than most bipolar technologies in these categories. On the other hand, I^2L is at a definite disadvantage to both bipolar and MOS technologies in terms of neutron damage susceptibility and noise immunity. All of the microcircuit technologies are capable of performance over the full military operating temperature range (-55 to +125°C) with the exception of n-MOS, which is generally restricted to 0 to 70°C operation. In general, the temperature design problems are most critical for bipolar technologies at low temperatures and most critical for MOS technologies at high temperatures.

For the trade-off analysis, the "four" mask, epitaxial form of I^2L can be defined as the commercial "baseline". Evaluations have been conducted by many laboratories to determine electrical performance with design variations, and some data is also available on radiation effects of these structures. Two types of considerations are identified. The first is an increase in pre-irradiation design margins for the same degradation with radiation stress. In this case, hardness can be increased by the additional stress required to consume the additional design margin. An increase in design margin of some parameters, however, can degrade other performance parameters of the array and set up the conditions for a trade-off. For example, a geometry change to increase inverter gain will increase the design margin for neutron damage; but the same change can decrease switching response and speed-power product. The second case is a decrease in parameter sensitivity with radiation stress, even for the same initial design margin. An example would be modification in processing to harden oxide passivation layers, which may reduce long-term ionization effects with little effect on initial design margins. It is also possible to, in the best case, increase initial design margins and decrease radiation damage sensitivity. An example would be a decrease of npn transistor base width.

Table 1.1 Subjective Comparison of LSI Technologies

	TTL	S/C TTL	R/H TTL	ECL	IIL	PMOS	nMOS	CMOS	CMOS/SOS
cell density	-	0	- -	-	+ +	+	+ +	0	+ +
switching speed	0	+	+	+ +	0	-	0	-	+ +
static power dissipation	-	-	-	- -	+	0	+	+ +	+ +
dynamic power dissipation	+	+	+	+	+	0	+	- -	-
speed-power product	-	0	-	0	+ +	0	+	0	+ +
output drive capability	+ +	+	+	+	+	-	0	-	- -
noise immunity	+	+	+	0	- -	0	0	+ +	+ +
temperature range	+	+	+	+	+	0	-	0	-
neutron damage	+	0	+ +	+ +	-	+	+	+	+ +
long-term ionization damage	+ +	+	+ +	+ +	+	-	- -	-	- -
transient logic upset level	+	0	+	0	+	0	0	+	+ +
$\dot{\gamma}$ survivability	+	0	+ +	+ +	+	+	+	-	+
EPO damage	+	0	+	+	0	0	0	0	-

++ superior, + good, 0 average, - below average, -- weak

The overall conclusion of the trade-off evaluation is that radiation hardness improvements can be achieved in"baseline" I^2L, some of which require performance compromises. It is clear, however, that not all radiation hardness goals can be met by the baseline I^2L technology and advanced I^2L structures must be investigated to determine I^2L applicability in most severe application.

Results of the NWSC efforts show substantial promise in advanced I^2L structures obtained from both Harris Semiconductor and Hughes Semiconductor. Principal competition in evolving LSI technologies for commercial technologies is n-MOS and its evolution to CCD arrays. Application of n-MOS/LSI to military systems, however, seems discouraging because of the trend to optimize for performance rather than temperature range or radiation hardness. Principal competition to advanced I^2L for military applications is CMOS/SOS. It remains to be established, however, that CMOS/SOS is of sufficient commercial LSI base or hardness to long-term ionization effects for hardened system applications. In many ways, advanced I^2L and CMOS/SOS are similar as low-power LSI technologies, but are quite complementary in key aspects of performance limitations and radiation susceptibility.

SECTION 2

2.0 COMPARATIVE EVALUATION

A detailed quantitative evaluation between LSI technologies is a complex and demanding task. Performance parameters of the principal LSI technologies are reviewed to present a discussion of the relative trends in performance and to finally support the subjective comparison presented in the summary.

Electrical performance data on the LSI technologies was obtained from that published in standard product catalogs[42-51] and technical review articles.[15] Radiation effects data were obtained from published results of studies on commercial LSI arrays,[41,51,55] hardened microcircuits[54] and LSI test cells.[41,52]

2.1 Cell Density

Cell density is a critical LSI parameter which reflects component yield. For a wafer with spacially-distributed defects, increasing cell density can allow arrays of given complexity to be realized at greater yield.

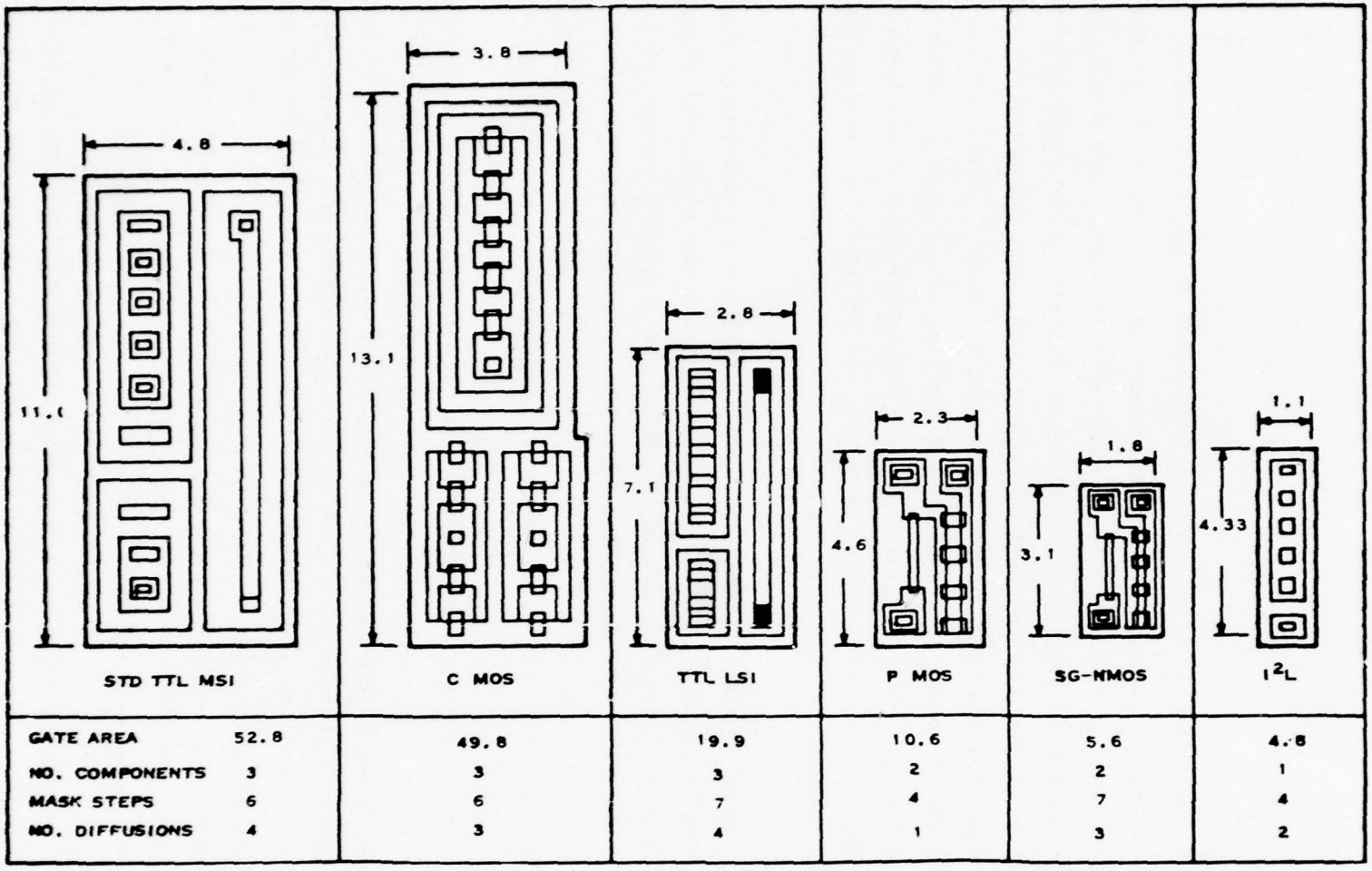
Two criteria can be considered as representative of cell density for a given LSI technology. The first is the geometry of a basic logic cell for state-of-the-art mask-layout rules. Typically this would be a basic inverter of nominal fan-out capability. A second criteria represen-

tative of cell density is the maximum complexity of available arrays. This has the advantage that practical limitations due to layout problems and overall processing complexities are implicitly included. The disadvantage of using maximum complexity of arrays as a criteria is the difficulty in defining an accurate measurement of element complexity for arrays of different functions and technology. As a practical matter, then, the comparison must be made of memory arrays of common function which gives a subtle advantage to those technologies that lend themselves to a larger number of regular, simple cells. This, then, may not be completely representative of irregular LSI logic arrays.

Logic cell geometries for several of the LSI technologies which are defined in Figure 2.1 [15] are representative of the logic cell criteria. Typical memory array complexities presently available are summarized in Table 2.1 as representative of the alternate criteria. Even for the memories, however, there are variations in coding and decoding, as well as variations in yield that are considered acceptable at a marketable price.

Considering these criteria, I^2L offers the highest cell density of all bipolar technologies and is comparable to that of silicon-gate n-MOS and CMOS/SOS which are comparable as the highest cell density of the MOS technologies. Specific variations between I^2L, n-MOS, and CMOS/SOS will depend principally on the cleverness of the design, allowable design margins in circuit and processing parameters, and the severity of environmental requirements. It is interesting to note that each of these high-density technologies are based on commercial products, and each, in turn, are highly susceptible to radiation effects.

For other bipolar technologies, Schottky-clamped TTL is of highest cell density with a slight edge over ECL, conventional TTL and radiation-hardened TTL. The principal reason that these bipolar



GATE AREA	52.8	49.8	19.9	10.6	5.6	4.8
NO. COMPONENTS	3	3	3	2	2	1
MASK STEPS	6	6	7	4	7	4
NO. DIFFUSIONS	4	3	4	1	3	2

Figure 2.1 Representative Logic Cell Geometries[15]

Table 2.1. Comparison of Cell Density from Memory Array Complexities.

	Static RAM	Dynamic RAM	ROM	Relative Density Array Size	Relative Density Cell Size
TTL [51]	64	no data	1.024	0.05	0.1
S/C TTL[51]	256	no data	2,048	0.2	0.2
ECL[46]	128	no data	256	0.1	-
I^2L[25]	no data	4,096	no data	1.0	1.0
p-MOS[45]	no data	1.024	16,384	0.5	0.45
n-MOS[45]	1,024	4,096	8,196	1.0	0.8
CMOS[48]	256	no data	no data	0.25	0.1
CMOS/SOS[50]	1,024	no data	no data	1.0	-

*No R/H TTL memory array is presently available as a standard product. It is assumed that the density would be slightly less than that of S/C TTL.

technologies are an order-of-magnitude less dense than I^2L is the area required by diffused or thin-film resistor elements. This is compounded in overall performance considerations by the increase in resistor geometry generally necessary in low-power designs making both objectives in contrast.

Improved cell densities in MOS technologies are the result of replacing load resistors by small-geometry active elements. In addition, CMOS/SOS elements can be closed-spaced on a dielectric substrate. The advantage of silicon-gate n-MOS is the exclusive use of high mobility n-MOS transistor elements and an effective two-layer cell interconnection capability. The relative decrease in density for p-MOS is due to the relatively low channel mobility. The cell density of bulk CMOS is limited by the relatively large number of elements required as well as the necessity of guard bands to prevent parasitic transistor effects. In general, however, all MOS technologies offer a substantial advantage in cell density compared to bipolar technology with the recent exception of I^2L. This advantage in cell density has been a major factor in the rapid development of MOS/LSI.

2.2 Electrical Switching Speed

The electrical switching speed of an array is determined by the signal propagation delay of the internal logic cells and by the time required to drive an external load. In addition, the nature of switching speed, as influenced by operating conditions, varies between LSI technologies. This variation with test condition can be defined into three categories:

1. fixed supply voltage, switching response such as TTL, S/C TTL, ECL, p-MOS, n-MOS,
2. variation of switching time with supply voltage such as CMOS, CMOS/SOS, and

3. variation of switching time with bias current such as I^2L where in addition in each case, there is a variation in each case with specified load.

Typical switching times (i.e., propagation delay) are summarized in Table 2.2 for the variety of LSI technologies. For the TTL technologies the switching time varies with the design parameters as reflected by the nominal, -L and -H standard series. Similarly, the switching response of ECL arrays is a function of circuit design. The value quoted in Table 2.2 is representative of the Motorola 10,000 series which is a compromise between the fastest switching speed and power dissipation.

Electrical switching response of MOS/LSI arrays is a function of design for single-polarity (p- or n-MOS) or design and supply voltage for CMOS. In general, the switching time decreases with increasing supply voltage, but the nature of the circuit operation requires specific voltages for p-/n-MOS while CMOS can be operated over a wide range in supply voltage. Increasing the supply voltage also increases the output drive capability of a CMOS array; however, the supply voltage is limited by drain-source punchthrough of individual transistor elements.

Electrical switching response of I^2L is a function of the injector bias current. At low currents the speed-power product is constant. Therefore, 1 pJ I^2L will have a propagation delay of approximately 200 ns at a bias current of 1 μA per stage. At high bias currents, the switching response is limited by carrier storage time in the npn transistor element. The minimum propagation delay is on the order of 10 ns for "baseline" I^2L technology.

From the data presented in Table 2.2, bipolar technology generally has a switching speed advantage over the MOS technology. The overlapped exceptions are I^2L which is a relatively slow bipolar technology and CMOS/SOS which is the fastest of the MOS technologies.

Table 2.2 Summary of LSI switching response.

Technology	Propagation Delay	Load	Test Conditions
a. TTL: 54L	33 ns	50 pF/4kΩ	V_{cc} = 5 V
TTL: 54	10 ns	15 pF/400Ω	V_{cc} = 5 V
TTL: 54H	6 ns	25 pF/280Ω	V_{cc} = 5 V
S/C TTL: 54LS	10 ns	15 pF/2kΩ	V_{cc} = 5 V
S/C TTL: 54S	3 ns	15 pF/280kΩ	V_{cc} = 5 V
R/H TTL: R54L	45 ns	50 pF/4kΩ	V_{cc} = 5 V
R/H TTL: R54	10 ns	15 pF/400Ω	V_{cc} = 5 V
R/H TTL: R54H	8 ns	25 pF/280Ω	V_{cc} = 5 V
ECL	2 ns		V_{EE} = -5.2 V
I^2L	1 μs	C_L = 10 pF	I_{EE} = 1 μA
I^2L	20 ns	C_L = 10 pF	I_{EE} = 50 μA
I^2L	10 ns	C_L = 10 pF	I_{EE} = 1 mA
b. p-MOS	250 ns	C_L = 20 pF	+5 V/-12 V
n-MOS	100 ns		
c. CMOS	70 ns	C_L = 20 pF	V_{DD} = 5 V
CMOS	30 ns	C_L = 20 pF	V_{DD} = 10 V
CMOS	25 ns	C_L = 20 pF	V_{DD} = 15 V
d. CMOS/SOS	2 ns	ring counter	V_{DD} = 10 V
CD4007	4 ns	C_L = 2.8 pF	V_{DD} = 12 V
CD4007	25 ns	C_L = 30 pF	V_{DD} = 10 V

a. T.I. TTL Data Book for Design Engineers[51]
b. Intel Standard Products Catalog[45]
c. RCA COS/MOS Data Book[48]
d. NRTC CMOS System Study Report[54]

2.3 Power Dissipation

The power dissipation in an LSI array is to various degrees a function of cell design, clock rate (or frequency of operation) and output loading. For bipolar technologies the power dissipation is generally the same for either static or dynamic operation and determined by either the fixed circuit design or bias current. For p-/n-MOS technology, the power dissipation increases with increasing frequency of operation, but the static power dissipation (excluding dynamic-only arrays) is a significant fraction of the total. CMOS arrays, on the other hand, exhibit very low static power dissipation, but a strong variation of dynamic dissipation with frequency of operation and output load.

Logic cell power dissipation for the LSI technologies are summarized in Table 2.3 for static operation and operation at a clock rate of 1 MHz.

In general, the MOS technologies have an advantage in power dissipation over the bipolar technologies, with the dramatic exception of I^2L. The low power dissipation of I^2L and CMOS at low clock rates is particularly impressive. The principal difference is, however, that the low power operation of I^2L must be obtained by low bias and long switching times must be specified. With CMOS, the switching transistor time remains constant, but the total average power dissipation decreases with decreasing clock frequency.

2.4 Speed-Power Product

Because of the complexities in comparing switching speed and power dissipation between various LSI technologies, the product of power dissipation and switching speed has been used as a figure of merit. For most LSI technologies, this is a straightforward product of the static power dissipation and logic cell propagation delay.

Table 2.3. Summary of LSI Power Dissipation.

	Power Dissipation per Gate		Test Conditions
	Static	Dynamic	
TTL: 54L (ref.51)	1 mW		V_{cc} = 5 V
54	10 mW		V_{cc} = 5 V
54H	22 mW		V_{cc} = 5 V
S/C TTL: 54LS (ref.51)	2 mW		V_{cc} = 5 V
54S	19 mW		V_{cc} = 5 V
R/H TTL: R54L (ref. 51)	1 mW		V_{cc} = 5 V
R 54	10 mW		V_{cc} = 5 V
R54H	23 mW		V_{cc} = 5 V
ECL (ref.46)	25 mW		V_{EE} = -5.2 V
I^2L (ref. 24)	0.7 μW		I_{EE} = 1 μA
	40 μW		I_{EE} = 50 μA
	800 μW		I_{EE} = 1 mA
p-MOS(ref.45)	1 mW		
n-MOS(ref.45)	0.3 mW		Intel 2104
CMOS (CD4000B) (ref. 48)	5 μW	1.5 μW/kHz	V_{DD} = 5 V
	10 μW	6 μW/kHz	V_{DD} = 10 V
	15 μW	16 μW/kHz	V_{DD} = 15 V
CMOS/SOS (ref. 54)	12 μW	15 μW/kHz	V_{DD} = 12 V

The calculation becomes more complex, however, when the dynamic power dissipation dominates the static power dissipation. An additional question, common to all new low-power LSI, is accounting for the energy which must be committed to the external capacitive load. For a logic swing of 5 volts and a 20 pF output capacitance, the load energy is 250 pJ. This is a very significant energy in an LSI technology where the internal energy for information storage is comparable to or less than the load energy.

Speed-power products for the LSI technologies are summarized in Table 2.4.

2.5 Output Drive

Consideration of output drive and comparison of LSI is another complex situation. In general, either MOS or bipolar elements can be designed to drive virtually any microelectronic load. The practical restriction, however, is the total element geometry that can be committed to the output interface necessary. In MOS technologies, the output drain current of a transistor element can be expressed up to pinch-off as,

$$I_D = \frac{\mu\varepsilon_{ox}}{2t_{ox}} \cdot \frac{W}{L}\left[2(V_{gs} - V_t)V_{ds} - V_{ds}^2\right] \qquad (2.1)$$

With the minimum length of the channel restricted by mask tolerances and considerations of voltage breakdown, the output conductance is then proportional to the channel width. Increasing the channel width, however, increases the gate capacitance of the output stage and increases the capacitance load on the internal logic cell. This increase in capacitance has a first-order effect on cell electrical switching response time.

The output conductance of MOS transistor elements is proportional to the channel mobility. Thus, n-channel elements have an advantage of about a factor-of-three over p-channel elements due to the relative value of electron and hole mobility in bulk silicon. The decrease in carrier mobility

Table 2.4 Summary of LSI Speed-Power Products

TTL:[51] 54L	33 pJ	V_{CC} = 5 V
54	100 pJ	V_{CC} = 5 V
54HH	132 pJ	V_{CC} = 5 V
S/C TTL:[51] 54LS	19 pJ	V_{CC} = 5 V
54S	57 pJ	V_{CC} = 5 V
R/H TTL:[51] R54L	45 pJ	V_{CC} = 5 V
R54	100 pJ	V_{CC} = 5 V
R54H	173 pJ	V_{CC} = 5 V
ECL[46]	50 pJ	V_{EE} = -5.2 V
I^2L[24]	0.5 pJ	I_{EE} = 1 μA
	1.0 pJ	I_{EE} = 50 μA
	5.0 pJ	I_{EE} = 1 mA
p-MOS[45]	100 pJ	
n-MOS[45]	10 pJ	
CMOS*[48]	125 pJ	V_{DD} = 5 V , C_L = 0
	500 pJ	V_{DD} = 10 V , C_L = 0
	2400 pJ	V_{DD} = 15 V , C_L = 0
	750 pJ	V_{DD} = 5 V , C_L = 50 pF
	3000 pJ	V_{DD} = 10 V , C_L = 50 pF
	8000 pJ	V_{DD} = 15 V , C_L = 50 pF
CMOS/SOS*[54]	72000 pJ	V_{DD} = 12 V

*Energy per switching transition

with increasing temperature is a significant design consideration for MOS arrays.

The output conductance of MOS elements on sapphire is somewhat less than that of bulk silicon due to a decrease in carrier mobility. This decrease in mobility may be as great as a factor-of-three for thin silicon films on a sapphire wafer. Research is still underway to improve the semiconductor quality of the silicon film.

For bipolar transistors, the output drive is typically that of a common-emitter collector current which can be expressed as,

$$I_C = qA_{jc}\left[-J_{es}(e^{\theta V_{be}} - 1) + J_{cs}(e^{\theta V_{bc}} - 1)\right]. \qquad (2.2)$$

The output current, again, is proportional to the area of the transistor within limits of sustaining current gain at the required current density and limitations of current crowding and high-level injection.

In general, for elements of comparable geometry, the output drive capability of bipolar elements is substantially greater than that of MOS elements. Of the bipolar technologies, I^2L is at a principal disadvantage because of the relatively low gain of the output inverter. Alternative output networks have been suggested which take advantage of high transistor gain, but these networks may involve isolation techniques that may introduce the possibility of latch-up. Also, as opposed to MOS technologies, the worst-case for bipolar elements is at low temperature where transistor gain is minimum.

For MOS technologies, n-MOS is most favorable for output conductance and CMOS/SOS the least favorable.

2.6 Noise Immunity

Noise immunity is one of the most complex parameters to define for any technology, as well as difficult to compare between technologies. It can be defined in a variety of ways and should be referenced to both the input terminal of a logic cell as well as to the power supply.

Referred to the input, the performance measure is the voltage, current, and/or energy required to induce a logic error with the logic element at the most sensitive bias of the 0- or 1-logic state. A similar definition can also be used at the power-supply terminal of the array. Regulation requirements at the power supply terminal should also be considered (but almost never are). That is, in a technology such as TTL, and CMOS, there is a significant power supply current transient during switching. The requirement for voltage regulation must them be consistent with power supply filtering to minimize the effects of the signal-induced current surges. It is suggested that for LSI arrays, power/supply ground noise immunity is more critical than input noise immunity. Just as for output conductance, it is necessary to specially design the interface cells of an array, even with trade-offs in element geometry and power dissipation. Generally, interface networks for both n-MOS and I^2L are designed to be essentially those of TTL and it is expected that interface noise immunity would be comparable. Power supply/ground noise immunity, however, is common to all internal logic cells of the LSI array.

In terms of voltage noise margin, as summarized in Table 2.5, CMOS (either bulk or SOS), with a noise margin approximately equal to 45 percent of V_{DD}, has a clear advantage over other bipolar and MOS technologies. The noise margins of n-MOS are essentially the same as that of TTL-compatible interfaces. For bipolar technologies, the voltage noise margin of ECL is somewhat less than that of TTL. There is no experimental data on the interfaced voltage noise margins of I^2L. Calculated results

Table 2.5. Noise Immunity Summary*.

Logic Family	D-C Bias	D-C Noise Margin V_{NL}	V_{HL}	Minimum Noise Energy E_{NL}	E_{HL}
TTL	5 V	1.2 V	2.2 V	1.7 nJ	1.0 nJ
CMOS	5 V	2.2 V	2.2 V	1.0 nJ	0.9 nJ
(bulk)	10 V	4.5 V	4.5 V	3.7 nJ	3.1 nJ
	15 V	6.8 V	6.8 V	7.2 nJ	8.5 nJ
I^2L	1 μA	0.6 V	0.06 V	25 nJ	0.3 pJ
	50 μA	0.65 V	0.06 V	0.72 nJ	0.6 pJ
	1 mA	0.75 V	0.06 V	0.49 nJ	5 pJ

* calculated from data in references 24, 48, 51.

indicate the worst-case noise margin as approximately 60 mV, which is significantly less than TTL and substantially less than CMOS.

Noise immunity considerations at the power supply terminal should include both the range of voltage or current which can be accommodated and the regulation requirements resulting from current or voltage pulses. In this case, TTL, ECL, p-MOS and n-MOS arrays require well regulated supply voltages (total variabion less than one volt). This is a significant requirement for TTL because of the power supply current surges that occur during a switching transient. On the other hand, both CMOS and I^2L have a high tolerance for variations in power supply voltage or current. In CMOS, a decrease in supply voltage results in a decrease in switching speed and noise margin but does not result in operational failure. Typically, the CMOS supply voltage can be selected from 5 to 15 V. In an I^2L array, operation is credible over a wide range of power supply bias currents (typically 1 μA to 1 mA per gate). As the power supply current is decreased, however, the electrical switching time is increased.

Noise immunity at signal interfaces can also be characterized in terms of the noise energy requried to cause a logic error rather than the noise voltage level. This noise energy can be defined as

$$E_N = V_N \cdot I_N \cdot t_p \tag{2.3}$$

where V_N and I_N are the noise voltage and current for a given pulse width, t_p, at the interface node as shown in Figure 2.2.

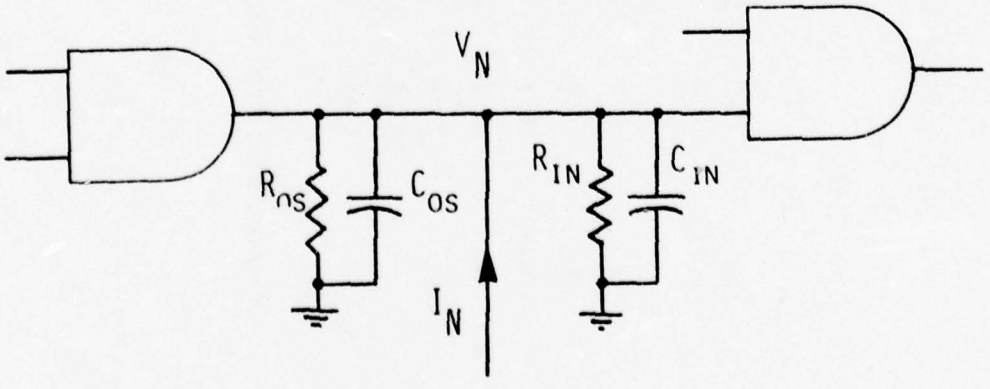


Figure 2.2. Gate Noise Immunity Characterization.

The driving point impedance at the interface node is essentially the parallel combination of the resistances and the sum of the non-linear capacitances. If the conductances are large compared to the capacitive susceptances, the expression for noise energy can be approximated as

$$E_N = \frac{V_N^2}{R_o} \cdot t_p \qquad (2.4)$$

where R_o is the combined driving-point resistance. Calculations in a Motorola application note using the resistive form of the energy equation are shown for TTL and CMOS technologies in Table 2.5. Corresponding calculated values for I^2L are shown and are based on a 1 pJ speed-power product technology.

Considered in terms of noise energy, the critical energy is approximately that committed to the storage of digital information in an array, which is reflected by the speed-power product of a technology. A low-power technology will tend to low noise immunity, and input and output interfaces must be transformed to high energy levels (such as TTL or CMOS). This has been the case in the evolution of silicon-gate n-MOS memories where internal noise margins are less than 200 mV, but input/output interfaces are at TTL levels.

2.7 Temperature Range

All bipolar LSI technologies, including I^2L, can be qualified over the full military temperature range (-55° C to +125° C). Similarly all MOS technologies can be qualified over the full range, but there is a tendency to design MOS/LSI for commercial rather than military requirements. As a result, virtually all silicon-gate n-MOS and CMOS/SOS arrays presently available are specified for operation over the limited range of 0° C to 70° C.

Design problems for MOS arrays are severe at high temperatures due to increases in junction leakage currents and the decrease in carrier mobility. Conversely, the design problems for bipolar technologies are most severe at low temperatures because of the decrease in transistor gain.

2.8 Radiation Effects

Quantitative comparison of LSI radiation susceptibility is complicated by variations in failure criteria implicit in available data. It is fairly easy, however, to identify the relative strengths and weaknesses for each technology for each aspect of the nuclear environment. A summary of approximate failure levels for each LSI technology is presented in Table 2.6.

Neutron displacement damage is a significant concern for all bipolar technologies and is of little concern for MOS technologies. The predominant effect in MOS damage will be ionizing radiation rather than neutron displacement damage alone. This is particularly true in CMOS/SOS where the semiconductor material is quite disordered initially and may be less valid for advanced MOS technologies that rely on high quality bulk semiconductor for low thermal leakage currents.

Of the bipolar technologies, neutron damage affects ECL, TTL, S/C TTL and I^2L in increasing order. The variations in susceptibility for ECL, TTL, and S/C TTL are small compared to potential design tradeoffs. Each can be designed for acceptable performance at neutron levels between 10^{14} and 10^{15} n/cm^2. The neutron damage susceptibility of I^2L is substantially greater with probable failure between 10^{13} and 10^{14} n/cm^2 for the baseline process. Detailed considerations for I^2L neutron damage effects and hardening techniques are presented in Section 3 of this report.

Table 2.6 Summary of LSI Radiation Hardness[55]

	Critical Neutron Fluence n/cm^2 (1 MeV)	Critical Total Ionization rads(Si)	Logic Upset Level rads(Si)/s	Electrical Pulse Overstress μJ @ 1 μs
TTL	5×10^{14}	1×10^{7}	$(1 - 5) \times 10^{8}$	∿ 13
S/C TTL	2×10^{14}	3×10^{6}	∿ 2×10^{8} * ∿ 5×10^{7} **	∿ 5
R/H TTL	1×10^{15}	1×10^{7}	5×10^{8}	no data
ECL	2×10^{15}	1×10^{7}	∿ 2×10^{8}	∿ 8
I^2L	3×10^{13}	$(0.1 - 1) \times 10^{6}$	$(0.1 - 1) \times 10^{9}$	no data
p-MOS	$> 10^{15}$	$(0.01 - 10) \times 10^{6}$	∿ 2×10^{8}	∿ 12
n-MOS	$> 10^{15}$	$(1 - 100) \times 10^{3}$	∿ 1×10^{8}	no data
CMOS	$> 10^{15}$	$(0.01 - 5) \times 10^{6}$	∿ 1×10^{9} * ∿ 5×10^{7} **	∿ 190
CMOS/SOS	$> 10^{16}$	$(0.01 - 1) \times 10^{6}$	$(0.5 - 10) \times 10^{10}$	∿ 0.1

*narrow pulse
**wide pulse
} possibility of radiation-induced latch-up

For the effects of long-term ionization, all MOS technologies have an intrinsic susceptibility substantially greater than bipolar technologies. Long-term ionization effects can be significant in low-power, high-performance bipolar microcircuits such as operational amplifiers, S/C TTL arrays without guard bands, and I^2L at low bias currents. In general, production-level bipolar technologies can withstand greater than 1 Mrad(Si) and hardened structures can perform well after an exposure of 10 Mrad(Si).

The general threshold of concern for commercial MOS is on the order of 10^4 rads(Si). Hardened bulk CMOS, can be consistently produced with high performance after a 1 Mrad(Si) exposure. Effort in the development of hardened CMOS/SOS has resulted in laboratory arrays of high performance for exposures of up to 1 Mrad(Si). On the other hand, commercial CMOS/SOS and n-MOS LSI still have high long-term ionization susceptibility because of design trade-offs which enhance electrical performance but compromise hardness.

The long-term ionization susceptibility of I^2L has not been well-defined. Some data on test structures suggests substantial susceptibility at exposure levels less than 100 krad(Si) at low bias currents, and other data on test structures suggests high performance at exposure levels of greater than 1 Mrad(Si).

Transient logic upset susceptibility of LSI is generally determined by the element isolation technique. Bipolar and static MOS arrays using junction isolation of elements on high lifetime (i.e., non-gold doped) substrates generally have logic upset levels on the order of 5×10^7 to 10^9 rads(Si)/s for narrow-pulse exposure ($\leq$ 30 ns), with a decrease of critical

dose rate with increasing pulse width to about an order-of-magnitude lower at wide pulse widths ($\gtrsim$ 2 μs). These technologies are also potentially susceptible to radiation-induced latch-up.

The logic upset level is increased substantially by dielectric isolation of the active elements. In bipolar TTL, the logic upset level can be increased to above 10^9 rads(Si)/s with decreased pulse width sensitivity. Dielectric isolation in CMOS/SOS further reduced the active volume for photocurrents. Logic upset levels of greater than 10^{10} rads(Si)/s have been realized for CMOS/SOS arrays.

The structure of I^2L, as well as some test data, suggests superior logic upset hardness for a non-dielectric isolated array. Logic upset levels of 10^9 to 10^{10} rads(Si)/s have been observed on flip-flop test cells. These data, however, are inconsistent with the 5×10^7 rads(Si)/s upset level measured by the T.I. microprocessor. It is suggested that good logic upset levels can be realized in an I^2L array, but it will not necessarily happen without design consideration. Similarly, I^2L should be latch-up free in a non-isolated, completely I^2L structure, but the use of high voltage (TTL or CMOS) interface networks and/or substrate isolation may be of concern.

Electrical pulse overstress susceptibility of LSI arrays is generally that of the interface networks and the power supply/ground terminals. At the input/output interfaces, the overstress susceptibility generally increases with decreasing semiconductor volume available for energy dissipation. Thus, minimum susceptibility is observed for large-geometry, junction-isolated interfaces, and maximum susceptibility is observed for minimum-geometry dielectric isolated interfaces. Measured failure levels for some of the technologies are summarized in Table 2.6. There is no data on electrical overstress susceptibility of I^2L, but the worst-case would be a minimum geometry output with a failure energy

on the order of 1 μJ for a 1 μs pulse. This is comparable to that of other low-power bipolar technologies and is somewhat better than that of CMOS/SOS. Harder input/output protection networds can be implemented in the CMOS/SOS array, but at a penalty of chip area and switching response time.

SECTION 3

3.0 PERFORMANCE/HARDNESS TRADE-OFF EVALUATION

No formal DoD program has been funded, at this time, to develop hardened I^2L. However, an AFAL procurement is anticipated to be started early in 1977. There have been many suggestions for I^2L hardening based on results of DNA and NWSC programs in the characterization of radiation effects on available test cells. This discussion will review possible hardening techniques in terms of possible performance gains or trade-offs. Yield and producibility are critical considerations, but cannot be included in this brief theoretical review. It is generally true, however, that yield and producibility decrease with the number and complexity of the processing steps.

3.1 Neutron Displacement Damage

The principal consideration in neutron damage susceptibility of I^2L is the effect on inverter fan-out. It is the nature of I^2L that the inverter can operate successfully at low current gain, but performance stops abruptly when the gain degrades below the fan-out. In baseline, commercial I^2L, the critical failure level has been reported as between 5×10^{12} to 5×10^{13} n/cm^2, depending on the bias current level and fan-out requirement.[23,24,28] I^2L is more susceptible than other bipolar or MOS LSI technologies to neutron damage.

The inverter gain (B) of the I^2L gate is a composite effect of the up-gain of the non-transistor element and the inverse gain of the lateral pnp transistor. As a first-order approximation, it can be assumed that the reciprocal of the inverter gain (1/B) increases linearly with neutron damage just as that of a discrete transistor (as shown in Figure 3.1). Inverter hardening can be accomplished by (1) increasing the unirradiated gain for the same (1/B) gain degradation rate, or (2) by decreasing the gain degradation rate, or (in the best case) by both.

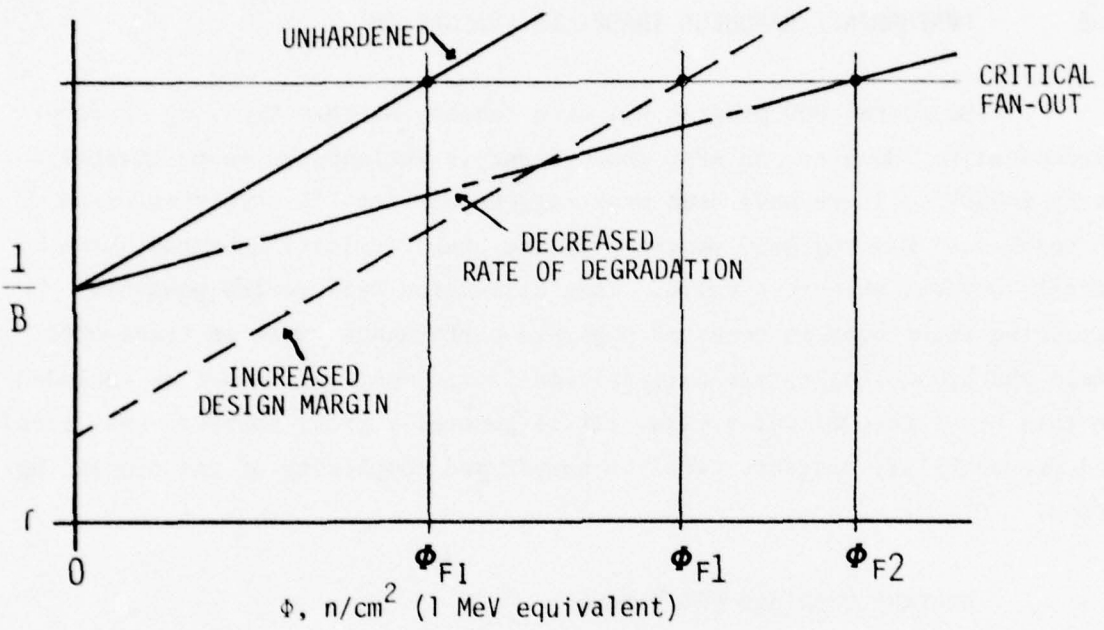


Figure 3.1. Assumed Nature of Gain Degradation.

Assuming that the inverter gain is dominated by the intrinsic up-gain of the npn transistor (i.e., back-injection of pnp transistor is negligible), the damage rate of the reciprocal gain can be defined as the increase in carrier recombination in the entire active emitter and base regions of the transistor. For the npn transistor in the up-mode, this volume is essentially that of the emitter n-region, the emitter-base depletion layer, and the active and inactive region of the p-base region. In practice, carrier recombination in the active base of the transistor is a very small fraction of the total carrier recombination.

This qualitative model can also be supported by a first-order analytical expression of gain in terms of geometrical and bulk semiconductor parameters which is,

$$B = \frac{A_{jc} D_n / W_{BN}}{(p_{no}/n_{po})\ A_{js} \cdot \frac{D_p}{W_{BP}} + A_{je} \cdot \frac{W_E}{\tau_p} + A_{jc} \frac{W_{BN}}{2\tau_n}} \qquad (3.1)$$

where, A_{jc} = npn collector area

A_{je} = npn emitter area

A_{js} = pnp base cross-sectional area

p_{no} = minority carrier density in the npn p-base region

n_{po} = minority carrier density in the n epitaxial layer

W_{BN} = npn transistor base width

W_{BP} = lateral pnp transistor base width

τ_p = minority carrier lifetime in n epitaxial layer

τ_n = minority carrier lifetime in p-base region.

Many of the principal mechanisms determining gain are represented in equation 3.1, but two dimensional effects, carrier transport in the npn overlap diode base region and injection level dependencies, are not included. On balance, the expression is a best-case representation of inverter gain.

With this qualitative model and first-order analytical expression, two means can be suggested to increase the initial gain while not affecting the rate of gain degradation. These are the effects of the transistor base width and n^+ collars around the periphery of the transistor. The inverter gain decreases with decreasing base width of the transistor. The presence of a retarding electric field in the base (typical

of the baseline process) effectively increases the base width over the geometrical value. Conversely, neutralizing the opposing base field (or creating an aiding field for the up-gain) will effectively decrease the transistor base width. The rate of gain degradation will not be influenced, however, because only a small fraction of the carrier recombination is in the active base region. The trade-off in this hardening approach is relatively slight. If a substantial aiding field is established for the up-gain, there will be a decrease in the down gain. A reasonable value of down-gain (typically greater than 10) is necessary to maintain low on-state output voltage. An increase in the on-state output voltage will lead to decreased noise margin and the possibility of current hogging. This trade-off is slight because the down-gain of an unirradiated inverter is typically greater than 100 and a significant margin is available.

The n^+ collars used to improve I^2L inverter gain are illustrated in Figure 3.2. Collars are used to reduce the hole injection from the sidewalls of the inverter the the substrate. This current is a loss for both the npn and the pnp transistor gains. The collar extends around the periphery of the inverter, except at the interface of the injector and npn p-base regions. There are three possible options in the use of collars: (1) no collars at all, (2) collars diffused to the depth of the collector diffusion and realized at the same time as the collector diffusion (i.e., no additional mask), and (3) collars diffused down to the emitter/injector junction (which requires an additional mesh and diffusion step). It has been shown that the inverter gain increases with the use of an n^+ collar, and the deeper collar has the greatest effect.[13] The use of the n^+ collar will be principally to increase the gain margin but will also have a less dramatic effect on the rate of gain degradation.

The trade-off in the use of n^+ collars is the increase in emitter depletion capacitance of the npn transistor. At low bias levels, the speed-power product of the inverter is directly proportional to the emitter

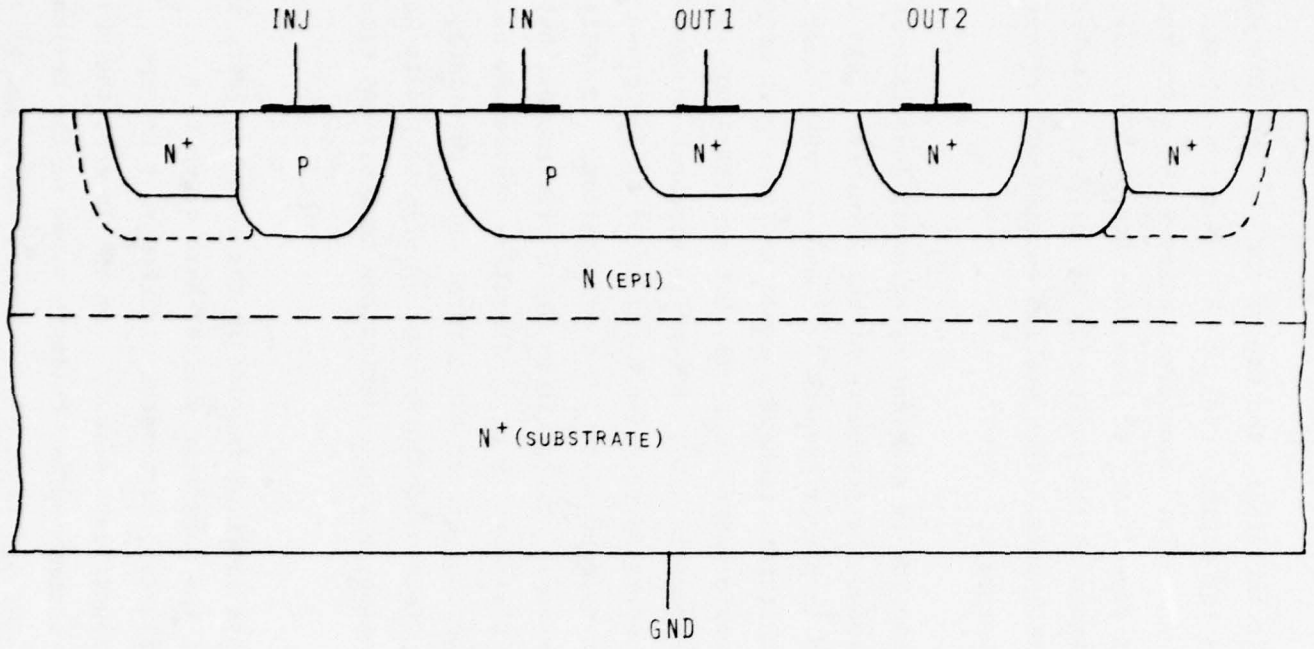


Figure 3.2 I^2L Inverter With N^+ Collar

depletion capacitance. In the limit, the use of the n^+ collars could be extended by increasing the doping level of the emitter n-region. The popularity of the $n\text{-}n^+$ epitaxial structures, however, suggests that this increase in the depletion capacitance is less than acceptable. Use of the n^+ collars also introduces the possiblity of collector-substrate shorts through mask misalignments. This problem becomes most severe for the deep n^+ collar structure.

An alternate solution to eliminating sidewall injection is the use of oxide isolation around the periphery of the inverter. This is employed in the Fairchild isoplanar process[25,26] and v-groove oxide isolation.[12] It is expected that this technique would increase gain margin with minimum electrical performance trade-off, but may introduce problems in long-term ionization susceptibility. Extensive research in hardened CMOS development has demonstrated relative hardness of oxides grown of 1-0-0 orientation silicon as opposed to 1-1-1 orientation. In collar dielectric isolation, the basic crystal is of 1-0-0 orientation, but the oxide over the interface periphery is not. Therefore, there may be an enhanced effect of trapped charge over the lateral oxide interface, over that expected from the surface oxide interface. Preliminary data is consistent with this observation, but no quantitative analysis has clearly identified a problem.

Considering other limiting factors in the inverter gain, the forward-biased current of the parasitic emitter-base diode is a significant effect. Similarly, the emitter efficiency of the npn transistor up-gain is a significant effect. For the former, the inverter gain can be increased by increasing the relative areas of the collector and emitter junctions of the npn transistor. In the limit, the effect of the parasitic diode would be minimized if the collector area were almost equal to the emitter area. The problem is, however, that it is desirable to minimize transistor area to increase cell density, yield, and effective

injection level for a given bias current. An additional consideration is the use of an extended base region to allow for metallization cross-overs. In a hardened design, that is one in which parasitic diode area is minimized, the use of extended base regions for cross-overs must also be minimized with a corresponding increase in the chip area required to realize a given LSI function.

Electrical performance of the I^2L inverter can also be improved by minimizing the width of the n-epitaxial layer under the npn emitter. This increases the gain of the inverter, reduces the switching delay time at high bias currents, and could reduce the rate of gain degradation.[38] The trade-off in minimizing the epitaxial width is principally one of process control. Contact of the n^+ substrate would result in inverters of high emitter depletion capacitance and high speed-power product. This may be a critical problem in realizing complex (greater than 1,000-gate) arrays.

Some of the hardened LSI structures have proposed minimizing the lateral pnp base width to minimize the gain degradation of the lateral pnp transistor. The baseline structure, however, reflects the merged effects of the pnp transistor in the inverter gain. When the npn transistor is forward-bias, a component of base current is injected from the npn base-emitter junction to the injector-ground junction. This can be reflected in the gain equation (Equation 2.1). Decreasing the lateral pnp base width increases the initial gain of the pnp device but decreases the inverter gain. The effects of inverse pnp transistor gain, particularly as a function of injection level and displacement damage, have not been accurately defined.

All the hardening techniques discussed to this point are relatively straightforward variations of the baseline "commercial" I^2L technology. Techniques such as deep n^+ collars, oxide isolation, up-diffusion (to reverse the npn base electric field), and double-diffusion (to minimize

lateral pnp base width) all add additional processing steps with a probable increase in fabrication complexity and decrease in overall yield. The specific impact of any of these techniques has yet to be determined in the structure of an LSI array. The application of oxide isolation in the Fairchild Isoplanar 4096-bit dynamic RAM does, however, demonstrate feasibility as a commercial LSI product.

An alternative approach to I^2L hardening is to make basic changes in the structure of the device. One of these presently proposed is substrate-fed-logic.[20,36] The basic structure of the substrate-fed I^2L inverter is shown in Figure 3.3. The principal change is the use of a p-substrate as the injector. This allows an increase in the injector area facing the npn emitter junction and allows the potential for a narrow-base pnp structure. A first-order analysis of the structure leads to

$$B = \frac{A_{jc}}{A_{je}} \cdot \frac{D_n/W_{BN}}{\frac{W_{BN}}{2\tau_n} + \frac{p_{nE}}{n_{pB}} \frac{D_p}{W_{BP}} + \frac{W_{BP}}{2\tau_p}} \qquad (3.2)$$

as an expression for inverter gain. Parameters are as defined previously in Equation 3.1 for the baseline structure. This expression includes the effect of the one-dimensional inverter and the parasitic pnp transistor. Each semiconductor region is considered as uniformly doped (i.e., effects of built-in electric fields are not included).

To get an analytical estimate of neutron damage suceptibility, lifetime degradation can be induced by assuming,

$$\frac{1}{\tau_n} = \frac{1}{\tau_{ni}} + \phi K_n$$

and

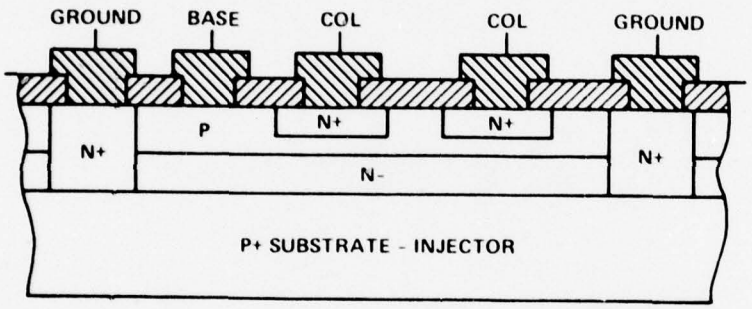


Figure 3.3 Substrate-Fed I^2L Structure[36]

$$\frac{1}{\tau_p} = \frac{1}{\tau_{pi}} + \phi K_p \tag{3.3}$$

where K_n and K_p are the lifetime damage constants. Substituting Equation 3.3 into Equation 3.2, the damage-inclusive inverter gain can be expressed as

$$\frac{1}{B}(\phi) = \frac{1}{B_i} + \frac{W_{BN}K_n}{2D_n} + \frac{p_{nE}}{n_{pB}} \cdot \frac{W_{BN}W_{Bp}K_p}{2D_n} \cdot \phi \tag{3.4}$$

where

$$\frac{1}{B_i} = \frac{p_{nE}}{n_{pB}} \cdot \frac{W_{BN}}{W_{Bp}} \cdot \frac{D_n}{D_p} + \frac{W_{BN}^2}{2 D_n \tau_{ni}} +$$

$$\frac{p_{nE}}{n_{pB}} \cdot \frac{W_{BN}\, W_{BP}}{2D_n\, \tau_{pi}} \quad . \tag{3.5}$$

Numerical evaluation of the analytical expression suggests a sensitivity to the relative doping levels in the emitter and base regions, as well as to the pnp transistor base width. However, as the inverter gain is improved by doping the emitter more heavily than the base, the rate of gain degradation decreases, supplementing the increase in design margin. For example, if the emitter is doped more heavily by a factor of 10, the unirradiated inverter gain is approximately 76 and is approximately 24 after exposure to 10^{14} n/cm^2.

Substrate-fed I^2L logic cells have been fabricated by Harris Semiconductor. Results of characterization on these test cells indicate initial inverter gains of 25, and gains of 5, following exposure to 3×10^{14}n/cm^2.[36] The feasibility of these structures has yet to be

demonstrated, however, as MSI/LSI arrays. Questions of performance and yield have yet to be answered. In the results presented, there was also a substantial decrease in gain with increasing injection level.[36]

Short-term annealing effects following pulsed neutron exposure have not been well defined in terms of LSI performance effects. From basic semiconductor device studies, the effective damage is greatest at short times and low carrier injection levels. Considering the injection level dependence, it is expected that effects in I^2L would be approximately the same as those in TTL, S/C TTL, or ECL. Operation of I^2L at low bias currents should be considered carefully, however, because of low average injection level, relatively long switching times and relatively narrow margins in transistor gain.

3.2 Long-term Ionization Damage

Long-term ionization damage effects have been characterized on test structures of several manufacturers by several investigators. Reported results however, are somewhat inconsistent.[19,23,24] The basic reason for these inconsistencies has not been identified. It seems reasonable to assume that the effect must be an increase in surface recombination velocity caused by radiation-induced positive charge trapped at the silicon-silicon-dioxide interface. The observed sensitivity at low bias currents suggests additional recombination at the surface of the emitter-base depletion region.

In evaluation of the inverter gain, one of the principal uncertainties is the recombination at the unmetaled surface of the npn base and injector p-regions. Numerical analysis by Jaeger,[30] suggests that the non-uniform doping of the p-region as formed by diffusion establishes a built-in

base field that restrains carriers away from the surface. As a result, the surface recombination has little effect on inverter gain. It is possible, then that shallow, sharply non-linearly doped structures would be less susceptible to long-term ionization effects than deeper, more uniformly doped structures. Substantial effort is necessary to clearly understand long-term ionization effects for bipolar technology in general and for I^2L specifically.

Structures and modifications of baseline I^2L suggested for hardening are exclusively concerned with neutron damage effects. Those modifications to increase the initial design margin will generally improve overall hardness. One exception to this may be oxide-isolated I^2L, as suggested from limited data on Fairchild test cells.[52] In oxide isolation the oxide sidewalls result in an oxide layer over the junction depletion layer at a 1-1-1 silicon orientation. Results on studies of MOS structures suggest a higher susceptibility for oxides grown over 1-1-1 silicon as opposed to those grown over 1-0-0 silicon as on the surface of the chip. Experimental results on the isoplanar test chips also show a susceptibility somewhat greater than that observed on baseline test cells.

Conversely, substrate-fed I^2L should be somewhat less susceptible to long-term ionization effects than baseline I^2L. There would be little difference in the inverter gain degradation, but, because the injector junction is essentially buried, the degradation in pnp gain should be less severe. Limited data published suggests this result.[36]

3.3 Transient Photoresponse

There is little data available on the logic upset level of I^2L logic cells, and no quantitative analysis to identify the failure mechanism in observed results. The first-order effect is

addition of junction photocurrents to the normal injector bias current. Logic upset, in this case, would be approximately the same as that of logic failure at high bias currents. At high bias currents, the inverter and lateral pnp gains tend to decrease due to high-injection level effects and/or voltage drops in the bulk semiconductor. If this is the case, the baseline structure could be hardened by optimizing design parameters for high-current operation. As usual, however, there will be trade-offs involved. For example, increasing doping levels will increase junction capacitances and will decrease the speed-power product that reflects operation at low bias currents.

In a practical baseline I^2L LSI array, operation at high bias currents can also be limited by the voltage drop along the injector rails. Hardening, then, would require constraints in layout to limit the length of the rails and would probably increase the size of the chip required for the same function.

No data is available on the transient photoresponse of substrate-fed logic arrays. The change in structure will substantially reduce the emitter-base photocurrent of the npn transistor, but the net result of this is not clear. The logic upset level could be reduced from that observed in baseline test structures.

3.4 Electrical Pulsed Overstress Damage

The principal concern for electrical damage is at the input and output signal interfaces. The power supply and ground terminals should not be particularly susceptible because of the large number of elements connected to the common pin, sharing the electrical overstress energy. For the input/output terminals, noise immunity and current drive requirements will require special interface network design, as discussed in Section 2. The signal interfaces will be TTL compatible

in voltage level, noise margin and overstress susceptibility. The trade-off involved is the chip area. In the worst-case, each input and output would require the chip area of a single input TTL gate (probably on the order of 20 $mils^2$ from Figure 2.1) and will require a significant increase in overall chip size necessary to realize an LSI function.

Assuming the use of minimum-geometry TTL interfaces on the I^2L array, the critical damage level would be on the order of $1\mu J$ for a $1\ \mu s$ pulse-width. Increasing the geometry of the interface elements would realize further hardening.

3.5 General I^2L Design Considerations

The design of I^2L is substantially more difficult in an LSI array than that of test cell inverters and ring counters. The principal difficulty is that cell performance depends critically on the doping profile (vertical design) and the geometrical layout (horizontal design). This is in contrast to MOS layout which is essentially just horizontal design, or other bipolar technologies which are essentially just vertical design. Relatively simple MOS design rules, based on just geometry scaling, can readily be incorporated into computer-aided design programs and are of substantial advantage in standard cell design and LSI design verification.

Many of the one-dimensional vertical design considerations have been discussed (e.g., npn base width, n epi-layer thickness, and base doping profile). Carrier transport in the pnp transistor base is a vertical design problem for substrate-fed logic, and a geometrical design problem for "baseline" I^2L.

Design considerations which must be considered in practical I^2L LSI design include:

1. layout of inverter collector outputs,
2. injector rail layout,
3. gain variation with high-level injector effects,
4. current partitioning between common-input inverters
5. tolerance requirements to avoid surface breakdown.

Design of test chips for I^2L evaluation and development must contain structures representative of those in an LSI array in order to determine relevant performance and radiation hardness capabilities and limitations. Lateral voltage drops limit the base current available to remote collectors of the inverter and limit the effective injector current at the end of a long injector rail. The voltage drop along the injector rail is probably the more vexing design problem. It is tempting to simply minimize the voltage drop by continuously running metalization over the rail. This, however, increasing electron current from the injector-substrate junction to the contact and reduces the pnp current gain. As an alternative, the injector can be broken into small segments, but that requires an increase in the metalization contacts which is a potential yield loss.

Gain loss in transistor elements due to resistive voltage drops is compounded at high bias currents by carrier high injection effects. Because of the small geometry used in the transistor elements, high injector levels (i.e., the current which establishes a minority carrier density comparable to the majority carrier doping level) can be at bias currents between 10 μA and 100 μA injector current per gate. The decrease in inverter gain at "high" bias currents is a critical design parameter in that minimum switching times can be obtained only if sufficient gain is retained at higher bias currents.

The final design problem is that which results when two or more

inverters are driven from a common voltage source. In this case, the input current will be preferentially partitioned to the inverter of lower input voltage and away from inverters of higher input voltage. The net result is a decrease in the worst-case gain capability of the overall inverter chain.

An additional difficulty of I^2L design is the relatively uncontrolled lateral diffusion of impurities laterally from a oxide cut. This under-diffusion determines the effective spacing of the injector and p-base regions as well as the spacing of the n^+ collectors and the n^+ collar around the inverter. As a practical matter, one of the major yield-limiting failure modes in I^2L is low breakdown voltage between the n^+ collector and the n^+ collar. By design, the n^+ collar must be in contact with the p-base region. Excessive under-diffusion, by either the collar or collector will reduce the collector-ground breakdown voltage to less than V_{BE} and will result in a functional failure.

SECTION 4

4.0 TRENDS IN LSI TECHNOLOGY EVOLUTION

Developments in LSI technology are inevitably motivated to improve performance, increase functional complexity, and decrease array cost. It has generally been the nature of this evolution during the past ten years, that the progress has also resulted in improving microcircuit hardness. There are indications now, however, that this is no longer true.[57] In this discussion, some of the trends in LSI technology will be presented in terms of performance and radiation hardness.

4.1 n/MOS, CCD Technologies

The use of small-geometry charge-controlled elements is a major influence in the realization of very complex LSI arrays. Silicon-gate n-MOS transistor elements with low threshold voltage (typically 0.5 to 1.5 volts) offer high performance for minimum geometry. Using n-MOS technology is particularly effective in realizing complex random-access memories. Memory complexities of 16 k-bits are at the state-of-the-art and 64 k-bit memories are expected in the near future.

CCD technology uses charge transfer between high density elements either at or just below the semiconductor surface. The nature of CCD array is particularly attractive for long serial memories, correlators, and image sensors. The application of CCD's as correlators and image sensors shows great promise.

In terms of radiation effects, however, the evolution of n-MOS and CCD technology has decreased hardness. Research in development of hardened CMOS is directly applicable, but involves trade-offs which are not generally considered in "commercial" LSI arrays. This is particularly apparent in presently available dynamic n-MOS 4k memories. These arrays are specified for operation over a limited temperature range (0 to 70° C) and damage susceptibility to long-term ionization effects consistently falls below 10 krads(Si). Unfortunately these limits restrict application of this commercial technology to military systems of modest radiation level requirements. This situation will probably continue for some time because, based on array complexity, n-MOS and CCD technologies are the leaders in commercial LSI technology.

4.2 Silicon-gate Bulk CMOS

Electrical performance of bulk CMOS can be improved with the use of amorphous silicon gate electrodes and minimum channel widths for the transistor elements. The use of silicon gates allows decreased threshold voltages for the elements and an overall increase in cell density because of reduced geometry and more flexibility in cell interconnection. Because of the nature of silicon gate processing, however, it is necessary to expose the critical gate $Si-SiO_2$ interface to more high temperature processing than that of aluminum gate CMOS. These high temperature processing steps tend to increase the threshold voltage shifts resulting from long-term ionization exposure. Minimizing the radiation-induced threshold voltage shift is particularly critical because of the low initial threshold voltage.

Low initial threshold voltages are also necessary in narrow-channel CMOS because of restrictions on the maximum supply voltage. With the narrow channel, the transistor elements are more susceptible to voltage breakdown by drain-source punch-through. Also with the increase in cell

density, the potential for electrical and radiation-induced latch-up becomes more significant. Gold-doping can be used to reduce the bulk semiconductor lifetime to minimize the latch-up susceptibility.[56] The gold-doping, however, will decrease the junction breakdown voltage and cause further concern for operation at maximum supply voltage.

In summary, narrow channel silicon gate CMOS offers potential for performance improvement with more sophisticated processing. Because of the nature of the silicon-gate processing, tighter gate threshold voltage requirements, and breakdown voltage effects, the hardening effort required will be substantially greater than that required of aluminum-gate bulk CMOS.

4.3 CMOS/SOS

Considering all MOS/LSI techniques, maximum performance in terms of switching speed, speed-power product, and power dissipation has been demonstrated by CMOS/SOS. Evolution of CMOS/SOS has been heavily supported by DoD for potential application in military avionic, satellite, man-pack communication and missile systems; however, commercial evolution of the technology does not have a wide base in the semiconductor industry. Maximum performance in CMOS/SOS can be realized with the use of minimum geometry elements, silicon gate conductors, and transmission gates. This evolution is inconsistent with maximizing the hardness of arrays. The nature of silicon gate processing exposes the gate oxide to high temperature stress as discussed for narrow-channel bulk silicon-gate CMOS. The use of transmission gates leads to unfovorable bias on the p-channel transistor. This bias condition can be relieved by biasing the body of the transistor, but with a sacrifice in gate density.

Specifically comparing CMOS/SOS to I^2L as evolving LSI technologies, a principal question is considering potential support of hardened I^2L. The

principal strengths of CMOS/SOS are:

1. electrical switching response,
2. low static power dissipation,
3. small logic cell area,
4. readily defined design rules for computer-aided design
5. low neutron damage susceptibility and
6. low photocurrent susceptibility.

The principal weaknesses of CMOS/SOS are:

1. expense of the starting material,
2. high defect density of the thin silicon film,
3. limited output drive capability,
4. high susceptibility to long-term ionization effects, and
5. high susceptibility to electrical pulse overstress damage.

On the other hand, the principal strengths of I^2L are:

1. low power operation,
2. low speed-power product,
3. high cell density,
4. low cost, high yield at LSI complexities,
5. low long-term ionization damage susceptibility, and
6. low photocurrent susceptibility.

The principal weaknesses of I^2L are:

1. complex design rules which complicate computer-aided design application,
2. limited electrical switching speed,
3. low electrical noise margin, and
4. high susceptibility to neutron displacement damage effects.

In terms of military applications, the principal concern of CMOS/SOS is the long-term ionization damage susceptibility, and the principal concern of I^2L is neutron damage susceptibility. With some development in process sensitivity evaluation and hardness assurance, both technologies are applicable for systems of modest radiation-hardening requirements. For system requirements of high ionization and low neutron levels, it would seem that effort in I^2L hardening could realize satisfactory arrays of minor variation from the broad-based commercial product. For very severe radiation hardening requirements, the relative effort in CMOS/SOS hardening from this point (based on an already substantial effort) is probably less than that required for I^2L. At this time, the long-term ionizing susceptibility of CMOS/SOS has been decreased by two orders of magnitude through DNA and SAMSO hardening. It seems reasonable to expect that research effort in I^2L can reduce I^2L neutron damage susceptibility.

Relative commercial support for CMOS/SOS and I^2L technologies will be determined by forces much broader than DoD procurement. The options for military systems are generally the selection of the best available from the overall technology resource. Maintenance of a specific LSI technology exclusively for hardened systems is a viable, but expensive, option and should be minimized.

SECTION 5

5.0 CONCLUSIONS

Integrated-injection logic is a real, evolving LSI technology of sufficient performance, cost, and realizability in very complex functions to assure potential military system applications. The present state-of-the-art is still one of unrealized potential, and the broad commercial technology base expected is probable, but not obvious. It is extremely unlikely that I^2L will displace many of the existing bipolar and MOS LSI technologies. Emitter-coupled logic and CMOS/SOS technologies are the principal competitors for high-speed arrays. The principal competitor for very dynamic large memories is n-MOS and CCD technology. CMOS is of particular advantage in systems that can exploit the very low static power dissipation. Application for I^2L seems particularly strong in very complex digital LSI arrays which must operate at low chip power dissipation at moderate, continuous clock rates.

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